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Confirmation No. 2306

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appellant:	AVERY *et al.*	Examiner:	Tu, C.
Serial No.:	10/796,480	Group Art Unit:	2138
Filed:	March 8, 2004	Docket No.:	US030080 US
Title:	CIRCUIT CONFIGURATOR ARRANGEMENT AND APPROACH THEREFOR		

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence and the papers, as described hereinabove, are being transmitted via facsimile-Formal Entry, to the attention of the Examiner at Commissioner for Patents, MAIL STOP APPEAL BRIEF, P.O. Box 1450, Alexandria, VA 22313-1450, on June 5, 2007.

Facsimile No.: 571 273-8300

By: Kelly J. Ledin

AMENDED APPEAL BRIEF

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Customer No. 65913

Dear Sir:

In response to the Notice of Defective Appeal Brief dated May 16, 2007, this is an Amended Appeal Brief submitted pursuant to 37 CFR § 41.37(d) for the above-referenced patent application.

This Amended Appeal Brief reflects changes only to Grounds of Rejection portion (*i.e.*, the listing of claims in the second grounds of rejection on appeal has been amended). Apart from the Grounds of Rejection portion (and this cover page), this brief duplicates the Appeal Brief filed on February 28, 2007.

Although no fee is believed to be necessary, authorization is given to charge/credit Deposit Account No. 50-0996 (NXPS.216PA) for any necessary fees/overages in support of this filing.

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I. Real Party In Interest

The real party in interest is NXP Semiconductors. The application is presently assigned of record, at reel/frame nos. 016759/0451 to Koninklijke Philips Electronics, N.V., headquartered in Eindhoven, the Netherlands. We have been authorized by both the assignee of record and NXP Semiconductors to convey herein that the entire right, title and interest of the instant patent application has been transferred to NXP Semiconductors.

II. Related Appeals and Interferences

While Appellant is aware of other pending applications owned by the above-identified Assignee, Appellant is unaware of any related appeals, interferences or judicial proceedings that would have a bearing on the Board's decision in the instant appeal.

III. Status of Claims

Claims 1-29 stand rejected and are presented for appeal. A complete listing of the claims under appeal is provided in an Appendix to this Brief.

IV. Status of Amendments

No amendments have been filed subsequent to the Office Action dated October 13, 2006.

V. Summary of Claimed Subject Matter

Commensurate with independent claim 1, an example embodiment of the present invention is directed to a circuit configurator arrangement for use in controlling routing circuitry having configurable test signal routing paths with controllable switches 115 therein for coupling test signals between dedicated test-signal circuitry and a target circuit device 110 (*see, e.g.*, Fig. 1; paragraphs 0030 and 0032). The circuit configurator arrangement includes a test-signal sense circuit 126 to detect test signals carried by at least one of the test signal routing paths and a switch-control interface circuit to control the controllable switches 115 (*see, e.g.*, Fig. 1; paragraphs 0032 and 0033). The circuit configurator arrangement further includes a control logic circuit to send control signals to the switch-control interface

circuit, in response to the detected test signals carried by said at least one of the test signal routing paths, and therein control routing of test signals in the configurable test signal routing paths (*see, e.g.,* Fig. 1; paragraphs 0030, 0032 and 0033).

Commensurate with independent claim 14, another example embodiment of the present invention is directed to a circuit configurator arrangement for use with a configured circuit 110 having a plurality of controllable switches 115 communicatively coupled between at least two JTAG test nodes (112, 114, 116 and 118) on JTAG signal paths and target circuit devices (150 and 160) along the JTAG signal paths (*see, e.g.,* Fig. 1; paragraphs 0030, 0032 and 0033). The circuit configurator arrangement includes a communications port 130 to accept control inputs from a user interface 140 via a communications link and to provide output data to the user via the communications link, a test-signal sense circuit 126 to detect JTAG test signals carried by at least one of the test signal routing paths, and a memory 122 having computer-executable code (*see, e.g.,* Fig. 1; paragraphs 0031 and 0033). The circuit configurator arrangement further includes a programmable microcontroller 120 communicatively coupled to the configured circuit 110, the communications port 130 and the test signal sense circuit 126, wherein the computer-executable code, when executed, causes the microcontroller 120 to control the controllable switches 115 for coupling JTAG test signals to the target circuit devices (150 and 160) in response to test signals sensed by the test-signal sense circuit 126, and to monitor operational characteristics of the configured circuit 110 and output data to the user interface 140 in response to the monitored operational characteristics (*see, e.g.,* Fig. 1; paragraphs 0033 and 0035).

Commensurate with independent claim 23, another example embodiment of the present invention is directed to a configurator circuit for use in a prototype arrangement of inter-connectable circuit boards (*e.g.,* 800), each of the inter-connectable circuit boards having JTAG test signal routing switches 801-814, at least two JTAG circuit paths and JTAG input/output (I/O) test nodes (830, 832, 834 and 836) for passing JTAG test signals to and from other inter-connectable circuit boards (*see, e.g.,* Fig. 8; paragraphs 0050 and 0052). The configurator circuit includes a memory 845 to store data including computer-executable code and a microcontroller 840 on a first one of the inter-connectable circuit boards 800 and communicatively coupled to the memory (*see, e.g.,* Fig. 8 and paragraph 0050). The

computer-executable code, when executed, causes the microcontroller 840 to monitor the JTAG I/O test nodes (830, 832, 834 and 836) to detect connectivity to another inter-connectable circuit; and automatically configure the JTAG test signal routing switches 801-814 in response to the JTAG I/O test node monitoring for routing JTAG test signals along a JTAG circuit path on at least the first one of the inter-connectable circuit boards 800 (*see, e.g.*, Fig. 8 and paragraph 0052). The configurator circuit further includes a communications link 848 to communicate control inputs from a user interface device to the microcontroller 840 and to communicate outputs from the microcontroller to the user interface, the microcontroller being operable in response to the control inputs (*see, e.g.*, Fig. 8 and paragraph 0051).

Commensurate with independent claim 29, another example embodiment of the present invention is directed to a circuit configurator arrangement for use in controlling routing circuitry having configurable test signal routing paths with controllable switches 115 therein for coupling test signals between dedicated test-signal circuitry and a target circuit device 110 (*see, e.g.*, Fig. 1; paragraphs 0030 and 0032). The circuit configurator arrangement includes test-signal sensing means 126 for detecting test signals carried by at least one of the test signal routing paths and switch-control interface means for controlling the controllable switches 115 (*see, e.g.*, Fig. 1; paragraphs 0032 and 0033). The circuit configurator arrangement further includes control logic means for sending control signals to the switch-control interface circuit, in response to the detected test signals carried by said at least one of the test signal routing paths, and therein control routing of test signals in the configurable test signal routing path(*see, e.g.*, Fig. 1; paragraphs 0030, 0032 and 0033).

As required by 37 C.F.R. § 41.37(c)(1)(v), a concise explanation of the subject matter defined in the independent claims involved in the appeal is provided herein. Appellant notes that representative subject matter is identified for these claims; however, the abundance of supporting subject matter in the application prohibits identifying all textual and diagrammatic references to each claimed recitation. Appellant thus submits that other application subject matter, which supports the claims but is not specifically identified above, may be found elsewhere in the application. Appellant further notes that this summary does not provide an exhaustive or exclusive view of the present subject matter, and refers to the specification,

including the appended claims and their legal equivalents, for additional example embodiments.

VI. Grounds of Rejection to be Reviewed Upon Appeal

1. Claims 1, 2, 4, and 8 stand provisionally rejected on the ground of obviousness-type double patenting over Avery *et al.* (U.S. Application No. 10/796,484).

2. Claims 14, 15, 16 and 17 stand provisionally rejected on the ground of obviousness-type double patenting over claims (12 & 13), 14, 15 and 17 of the co-pending Application No. 10/796,484.

3. Claims 23 and 26-27 stand provisionally rejected on the ground of obviousness-type double patenting over claims (19 & 23) and 21-22 of the co-pending Application No. 10/796,484.

4. Claim 29 stands provisionally rejected on the ground of obviousness-type double patenting over claims (12 & 13) of co-pending Application No. 10/796,484.

5. Claims 1-29 stand rejected under 35 U.S.C. § 112(2).

6. Claims 1-10, 13-14, 16-18, 22-26 and 29 stand rejected under 35 U.S.C. § 103(a) over Garreau (U.S. Patent No. 6,425,101).

VII. Argument

The provisional rejections on the grounds of obviousness-type double patenting are addressed at the end of this Argument section under item D, with the claim rejections under §§112(2) and 103(a) addressed first.

A. The Section 112(2) rejection of claims 1-29 is improper because the limitations referred to in the rejection are either widely accepted or have been removed from the claims.

The Section 112(2) rejection must be reversed because the terms upon which the rejections are based are widely accepted and implemented (thus well understood) and the specification provides ample description of the terms; the Office Actions of record have correspondingly failed to show or allege ambiguity in any of the claimed limitations in a manner consistent with M.P.E.P. § 2173.02.

The Section 112(2) rejection must also be reversed because certain limitations upon which the rejection is based are no longer present in the claims (*i.e.*, the Appellant has removed claim limitations upon which the rejections are based, yet the rejections have been maintained to these now non-existent claim limitations). Specifically, the Section 112(2) rejection of independent claims 1, 14, 13 and 29 based upon the use of the terms "adapted to," "adaptively" and "adapted for" must be reversed because these terms are no longer present in the independent claims (per an amendment filed 7/11/2006).

Regarding pending claims that recite terms including "adapted to," "adaptively" and "adapted for," all of these terms have come to be commonly used claim terms and are strongly supported in the specification. A brief review of the U.S. Patent Office's own database indicates that the term "adapted" has been used in the claims of tens of thousands of issued patents in recent years. Appellant's specification describes various example embodiments that may be implemented in connection with such limitations. For instance, the discussion in the specification in connection with FIG. 1 describes example embodiments directed to a communications link that is coupled (*e.g.*, adapted to communicatively couple as in claim 2) to a user interface by way of a communications port. Further referring to FIG.

1, an IC 110, memory 122, JTAG controller 124 and test signal sensing circuit 126 are all coupled (*i.e.*, communicatively) to a microcontroller 120.

Specifically regarding the Section 112(2) rejection of claim 9 with respect to limitations including routing JTAG signals on the routing circuitry and between the routing circuitry and an external circuit, several examples are described in Appellant's specification (*see, e.g.*, Figure 1; paragraphs 0033 and 0052). Generally, the art of JTAG and other circuit testing involves routing signals in a variety of manners and, as explained in the specification and shown in the figures, these examples are readily understood by one of skill in the art of test signals and related connectivity. For example, one of skill in the art would understand that the JTAG signals are routed "on the routing circuitry and between the routing circuitry and an external circuit" as claimed (*e.g.*, with signals passed not only on the routing circuitry itself but to an external circuit for testing). This external circuit use is not inconsistent with further supporting information as readily available from the Joint Test Access Group (JTAG), the usual name used for the IEEE 1149.1 standard entitled "Standard Test Access Port and Boundary-Scan Architecture" for test access ports used for testing printed circuit boards.

In view of the foregoing, the scope of the claims is ascertainable and therefore the Section 112(2) rejection of claims 1-30 is improper and must be reversed.

B. The Section 103(a) rejection of claims 1-10, 13-14, 16-18, 22-26 and 29 is improper because the cited Garreau reference fails to teach or suggest all of the claimed limitations.

The Section 103(a) rejection must be reversed because the cited portions of the Garreau reference (the sole reference relied upon for the rejection) do not teach or suggest all of the claimed limitations. For instance, the Examiner's acknowledges at page 7 of the Final Office Action that the Garreau reference "does not explicitly teach the controllable switches," yet the rejection provides no reference that teaches or suggests these limitations. Moreover, the Garreau reference does not teach a test signal sense circuit that detects the presence of test signals carried by routing paths to control the switching of signals on the paths as in the claimed invention (*see, e.g.*, each of the independent claims). These and other limitations are more particularly addressed below under claim subheadings.

Claims 1, 14 and 29:

Regarding independent claims 1, 14 and 29, and as further applicable to limitations in claim 23 argued separately below, the cited portions of the Garreau reference are unrelated to claimed limitations directed to detecting the presence of test signals (*e.g.*, to determine connectivity of test signal paths) and routing test signals in response to the detected signals. Referring to claim 1 by way of example, test signal routing is controlled in response to the presence of test signals detected by a test signal sense circuit, using controllable switches that couple test signals between dedicated circuitry and a target circuit. This approach may, for example, be used to sense the connectivity of various circuit components such as ICs and the corresponding routing of test signals therebetween (*see, e.g.*, Appellant's specification in paragraph 0033). The Garreau reference fails to teach or suggest such limitations, in that the test signals are used to "assess whether the integrated circuit being tested is functioning properly" (*see, e.g.*, col. 4, lines 56-66) as indicated in the Final Office Action dated 10/13/2006, on page 12. That is, while Garreau's I/O lines 211-1 and 211-2 pass test signals that are used in analyzing the general function of circuits, Garreau does not teach or suggest that these signals are used to sense the presence or absence of test signals for routing purposes as in the claimed limitations. Garreau further does not teach that any routing is carried out in accordance with any sensed signals or circuit connectivity relating to the same as in the claimed limitations. Generally, it appears that the Examiner has misinterpreted the function and implementation of the claimed test signal sense circuit and corresponding routing, and in doing so has cited to unrelated portions of the Garreau reference that fail to teach or suggest the claimed limitations (*see, e.g.*, pages 12-13 of the Final Office Action dated 10/13/2006).

As indicated by the Examiner at page 7 of the Final office Action, Garreau also fails to teach or suggest limitations directed to controllable switches. In an apparent attempt to show teaching or suggestion of related claimed limitations, the Examiner has suggested that "Garreau's combination of a plurality of vertical data lines (402) and the plurality of the horizontal data lines (404) ... would have been the controllable switches." This suggestion is confusing as to whether the Examiner is proposing to modify the Garreau reference (*i.e.*, as

would be consistent with making the rejection under Section 103) or suggesting that these data lines correspond directly to the claimed limitations. Regardless, these cited horizontal and vertical data lines in the Garreau reference fail to teach or suggest controllable switches "for coupling test signals between dedicated test-signal circuitry and a target circuit device" and "a switch-control interface circuit to control the controllable switches" as in claim 1.

In view of the above and as applicable to limitations in each of the independent claims, the Garreau reference fails to provide teaching or suggestion of all of the claimed limitations, and the Section 103(a) rejection of claims 1, 14 and 29 must therefore be reversed.

Claim 23:

Regarding claim 23, the claimed limitations are directed to subject matter including inter-connectable circuit boards in a prototype arrangement with each circuit board including routing switches, with interconnectivity between the boards detected for analysis. That is, the circuit boards in claim 23 each include JTAG routing switches, and further include a configurator for controlling the switches. This approach facilitates the detection of external connected circuit boards, which in turn facilitates the passing of test signals between boards. Neither Garreau's master controller 202 nor the slave target device 206 includes test signal routing switches in the context of the claimed limitations or otherwise. The alleged switching (via switch 400) in the Garreau reference is separate from either the master controller 202 or the slave device 206. In short, Garreau's passing of test signals between an off-chip master controller 202 (including JTAG controller 210) and a slave target device 206 (including integrated circuits IC1-IC4) using a programmable switch (400) that is separate from either the controller 202 or the target device 206 has no correspondence to the claimed limitations. In this regard, Garreau's master controller 202 and slave target device 206 are not inter-connectable circuit boards in the context of the limitations in claim 23, as asserted in the Final Office Action dated 10/13/2006, on page 13. In this regard, the rejection of claim 23 must be reversed.

Claims 2-10, 13, 16-18, 22 and 24-26:

The Section 103(a) rejections of all of the dependent claims, including 2-10 and 13 (which depend from claim 1), claims 16-18 and 22 (which depend from claim 14), and claims 24-26 (which depend from claim 23), must also be reversed in view of the above discussion regarding the independent claim rejections. That is, where an independent claim is nonobvious under 35 U.S.C. 103, then any claim depending therefrom is nonobvious. *See, e.g., In re Fine*, 837 F.2d 1071 (Fed. Cir. 1988). In this regard, further discussion of the dependent claimed limitations is unnecessary as the rejections must be reversed in view of the above.

C. The Section 103(a) rejection of claims 1-10, 13-14, 16-18, 22-26 and 29 is improper because there is no motivation for modifying the Garreau reference.

Before addressing the lack of motivation, Appellant notes that the Examiner's rejection acknowledges on one hand that the Garreau reference "does not explicitly teach the controllable switches" but, on the other hand, asserts that "Garreau's combination of a plurality of vertical data lines (402) and the plurality of the horizontal data lines (404) ... would have been the controllable switches." As similarly discussed above in section B, the rejection is confusing as to whether the Examiner is modifying Garreau's combination of data lines or is suggesting that this combination of data lines is inherently the same as the claimed limitations, because no evidence has been cited in support of the proposed modification.

Regardless, the Section 103(a) rejection must be reversed because there is no motivation to "realize" (as suggested at page 7 of the Final Office Action) that Garreau's vertical and horizontal data lines (402 and 404) function as controllable switches and as the claimed limitations. The Examiner has cited no evidence supporting the assertion that Garreau's data lines directly correspond to, or could be modified to correspond to, the claimed limitations of the instant invention. For example, various example embodiments of the present invention are directed to a configured circuit having controllable switches (*see, e.g.*, claim 14) and inter-connectable circuit boards having configurable test signal routing switches (*see, e.g.*, claim 23). Appellant submits that one of skill in the art would not realize that the vertical 402 and horizontal 404 data lines of Garreau, which are separate from

Garreau's master controller 202 and slave target device 206, in any way correspond to the controllable switches of the claimed invention.

For the reasons discussed above, Appellant submits that the Section 103(a) rejection of claims 1-10, 13-14, 16-18, 22-26 and 29 is improper and must be reversed.

D. The Section 103(a) rejection of claims 1-10, 13-14, 16-18, 22-26 and 29 is improper because the rejection failed to apprise the Appellant of the nature of the rejections in failing to allege any specific correspondence to each claimed limitation.

The section 103(a) rejections must be reversed because the Examiner failed to show or allege correlation between the Garreau reference and the claimed limitations in a manner that accurately conveys the nature of the rejection to the Appellant as required by 35 U.S.C. § 132 and the M.P.E.P. While certain portions of the Garreau reference are discussed generally, there has been no explanation as to how the cited portions of the Garreau reference correspond to each of the claimed limitations. For instance, page 6 of the Final Office Action discusses the Garreau reference generally, but fails to mention any of the claimed limitations of the present invention (*e.g.*, a test-signal sense circuit, switch-control interface circuit or control logic circuit as in claim 1). The Examiner further acknowledges at page 7 of the Final Office Action that the Garreau reference "does not explicitly teach the controllable switches" and only offers that such limitations could be "realized" without citing any evidence or teaching or suggestion to do so. This discussion at pages 6 and 7 of the Final Office Action thus fails to provide any explanation as to how the cited portions of Garreau could teach or suggest any claim limitations. In this regard, Appellant has been unable to ascertain which portions of the Garreau reference the Examiner is relying upon as allegedly teaching or suggesting various claimed limitations. The rejections thus failed to adequately apprise the Appellant of the nature of the rejections such that the Appellant could address the propriety of the rejections; the Section 103(a) rejections must therefore be reversed.

E. The provisional rejection of claims 1, 2, 4, 8, 14-17, 23, 26-27 and 29 on the grounds of obviousness-type double patenting is improper because there is no correspondence between the claims and those of co-pending Application No. 10/796,484, and because the remaining claim rejections are overcome.

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The provisional rejection must be reversed because the claims are patentable distinct from those of co-pending Application No. 10/796,484. To maintain an obviousness-type double patenting rejection, the Examiner must largely comply with the same standards as those applicable to a Section 103 rejection. In this instance, the double-patenting rejection is improper because the claims of co-pending Application No. 10/796,484 do not contain a test-signal sense circuit or a test-signal sense means as in the claimed invention. Accordingly, the rejection must be reversed. Moreover, pursuant to M.P.E.P. § 804, with the remaining rejections having been addressed and overcome for the reasons discussed above, the provisional rejection is improper and must be reversed.

VIII. Conclusion

In view of the above, Appellant submits that the rejections of claims 1-29 are improper. Appellant therefore requests reversal of the rejections as applied to the appealed claims and allowance of the entire application.

Authority to charge the undersigned's deposit account was provided on the first page of this brief.

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APPENDIX OF CLAIMS INVOLVED IN THE APPEAL
(S/N 10/796,480)

1. (previously presented) For use in controlling routing circuitry having configurable test signal routing paths with controllable switches therein for coupling test signals between dedicated test-signal circuitry and a target circuit device, a circuit configurator arrangement comprising:

a test-signal sense circuit to detect test signals carried by at least one of the test signal routing paths;

a switch-control interface circuit to control the controllable switches; and

a control logic circuit to send control signals to the switch-control interface circuit, in response to the detected test signals carried by said at least one of the test signal routing paths, and therein control routing of test signals in the configurable test signal routing paths.

2. (Original) The circuit configurator arrangement of claim 1, further comprising a communications link adapted to communicatively couple the control logic circuit to an external user-controlled device for passing reconfiguration-control signals to the control logic circuit, the control logic circuit being adapted to respond to the reconfiguration-control signals by sending control signals to the switch-control interface circuit for adaptively controlling the routing of the test signals in the configurable test signal routing paths.

3. (Original) The circuit configurator arrangement of claim 2, further comprising a memory adapted to store the reconfiguration-control signals for access by the control logic circuit, the stored reconfiguration-control signals, when executed, causing the control logic to send control signals to the switch-control interface circuit for adaptively controlling the routing of the test signals in the configurable test signal routing paths.

4. (Original) The circuit configurator arrangement of claim 2, wherein the communications link is further adapted for reporting characteristics of the configured test signal routing paths to the external user-controlled device.

5. (Original) The circuit configurator arrangement of claim 1, further comprising a memory adapted to store said control signals for access by the control logic circuit, the stored control signals, when executed, causing the control logic to send signals to the switch-control interface circuit for adaptively controlling the routing of the test signals in the configurable test signal routing paths.

6. (Original) The circuit configurator arrangement of claim 1, wherein the test-signal sense circuit is adapted to detect test signals passing between the configurable test signal routing paths and an external circuit and wherein the control logic circuit is adapted to adaptively control routing of test signal between the configurable test signal routing paths and the external circuit, in response to the detected test signals.

7. (Original) The circuit configurator arrangement of claim 1, wherein the dedicated test-signal circuitry includes a test-data input port adapted to receive test data, a test-data output port adapted to pass test data from the dedicated test-signal circuitry and a test-clock port.

8. (Original) The circuit configurator arrangement of claim 1, wherein the control logic circuit is programmed to control and monitor a plurality of operational characteristics of the configurable test signal routing paths.

9. (Original) The circuit configurator arrangement of claim 1, wherein the configurable test signal routing paths include a plurality of JTAG signal path switches adapted to route JTAG signals on the routing circuitry and between the routing circuitry and an external circuit, and wherein the control logic circuit is programmed to send the control signals to configure the plurality of JTAG signal path switches.

10. (Original) The circuit configurator arrangement of claim 9, wherein the control logic circuit is programmed to switch the plurality of JTAG signal path switches in response to reconfiguration-control signals received from an external user-controlled device.

11. (Original) The circuit configurator arrangement of claim 1, wherein the control logic circuit is adapted to monitor operational characteristics of the routing circuitry prior to power-up of the routing circuitry.

12. (Original) The circuit configurator arrangement of claim 1, wherein the control logic circuit is adapted to send control signals to the switch-control interface circuit and therein set the controllable switches, prior to power-up of the routing circuitry.

13. (Original) The circuit configurator arrangement of claim 1, wherein the control logic circuit is further adapted to control a JTAG controller for generating JTAG test signals and adaptively control the routing of the generated JTAG test signals in the configurable test signal routing paths.

14. (previously presented) For use with a configured circuit having a plurality of controllable switches communicatively coupled between at least two JTAG test nodes on JTAG signal paths and target circuit devices along the JTAG signal paths, a circuit configurator arrangement comprising:

a communications port to accept control inputs from a user interface via a communications link and to provide output data to the user via the communications link;

a test-signal sense circuit to detect JTAG test signals carried by at least one of the test signal routing paths;

a memory having computer-executable code; and

a programmable microcontroller communicatively coupled to the configured circuit, the communications port and the test signal sense circuit, wherein the computer-executable code, when executed, causes the microcontroller to control the controllable switches for coupling JTAG test signals to the target circuit devices in response to test signals sensed by the test-signal sense circuit, and to monitor operational characteristics of the configured circuit and output data to the user interface in response to the monitored operational characteristics.

15. (Original) The circuit configurator arrangement of claim 14, wherein the microcontroller is programmed to cause the test-signal sense circuit to monitor the JTAG test nodes using an interrupt routine for automatically detecting test signals at the JTAG test nodes.

16. (Original) The circuit configurator arrangement of claim 14, wherein the microcontroller is programmed to control the controllable switches for routing JTAG test data between the configured circuit and an external configured circuit, via the JTAG test nodes.

17. (Original) The circuit configurator arrangement of claim 14, wherein the microcontroller is adapted to control the controllable switches in response to control inputs received from the user interface via the communications port.

18. (Original) The circuit configurator arrangement of claim 14, wherein the circuit configurator arrangement is adapted to receive computer-executable code from the user interface via the communications port and to store the computer-executable code in the memory, the received and stored computer-executable code, when executed, causing the microcontroller to control the controllable switches.

19. (Original) The circuit configurator arrangement of claim 14, wherein the microcontroller is programmed to perform diagnostic testing on the configured circuit when the configured circuit is not powered and to report the results of the diagnostic testing via the communications port.

20. (Original) The circuit configurator arrangement of claim 19, wherein the microcontroller is programmed to report an error signal in response to the diagnostic testing indicating an error in the routing circuitry.

21. (Original) The circuit configurator arrangement of claim 19, wherein the microcontroller is adapted to perform diagnostic testing on timing circuits coupled to the routing circuitry by detecting clock frequency thereof and, in response to detecting an improper clock frequency, to report an error signal indicating a timing error.

22. (Original) The circuit configurator arrangement of claim 14, further comprising an analog-to-digital converter (ADC) coupled to the configured circuit and adapted for converting detected analog signals thereon to digital signals, the microcontroller being further adapted for reporting characteristics of the configured circuit in response to the digital signals.

23. (previously presented) For use in a prototype arrangement of inter-connectable circuit boards, each of the inter-connectable circuit boards having JTAG test signal routing switches, at least two JTAG circuit paths and JTAG input/output (I/O) test nodes for passing JTAG test signals to and from other inter-connectable circuit boards, a configurator circuit comprising:

a memory to store data including computer-executable code;

a microcontroller on a first one of the inter-connectable circuit boards and communicatively coupled to the memory, the computer-executable code, when executed, causing the microcontroller to:

monitor the JTAG I/O test nodes to detect connectivity to another inter-connectable circuit; and

automatically configure the JTAG test signal routing switches in response to the JTAG I/O test node monitoring for routing JTAG test signals along a JTAG circuit path on at least the first one of the inter-connectable circuit boards; and

a communications link to communicate control inputs from a user interface device to the microcontroller and to communicate outputs from the microcontroller to the user interface, the microcontroller being operable in response to the control inputs.

24. (Original) The configurator circuit of claim 23, wherein the computer-executable code, when executed, causes the microcontroller to monitor the JTAG I/O test nodes and, in response to detecting connectivity to another inter-connectable circuit via the monitoring, to set the controllable switches for routing JTAG test signals between the inter-connectable circuits.

25. (Original) The configurator circuit of claim 23, wherein the computer-executable code, when executed, causes the microcontroller to monitor the JTAG I/O test nodes and, in response to detecting that another inter-connectable circuit is not connected to a particular JTAG test node via the monitoring, to set the controllable switches for routing away from the particular JTAG test node.

26. (Original) The configurator circuit of claim 23, wherein the microcontroller is adapted to set the JTAG test signal routing switches in response to control inputs received from the user interface.

27. (Original) The configurator circuit of claim 23, wherein the computer-executable code, when executed, causes the microcontroller to perform an interrupt routine for monitoring the JTAG I/O test nodes.

28. (Original) The configurator circuit of claim 23, wherein the computer-executable code, when executed, causes the microcontroller to perform a data-polling routine for monitoring the JTAG I/O test nodes.

29. (previously presented) For use in controlling routing circuitry having configurable test signal routing paths with controllable switches therein for coupling test signals between dedicated test-signal circuitry and a target circuit device, a circuit configurator arrangement comprising:

test-signal sensing means for detecting test signals carried by at least one of the test signal routing paths;

switch-control interface means for controlling the controllable switches; and

control logic means for sending control signals to the switch-control interface circuit, in response to the detected test signals carried by said at least one of the test signal routing paths, and therein control routing of test signals in the configurable test signal routing path.

APPENDIX OF EVIDENCE

Appellant is unaware of any evidence submitted in this application pursuant to 37 C.F.R. §§ 1.130, 1.131, and 1.132.

APPENDIX OF RELATED PROCEEDINGS

As stated in Section II above, Appellant is unaware of any related appeals, interferences or judicial proceedings.